SEMICONDUCTOR DEVICE

AND

METHOD OF MANUFACTURING THE SAME

FIELD OF THE INVENTION

The present invention relates to a semiconductor device in which a semiconductor element is secured to a board and a method of manufacturing the same.

BACKGROUND OF THE INVENTION

Conventionally, semiconductor element chips (semiconductor elements; hereinafter, "chips") have been developed incorporating integrating transistors and an IC (integrated circuit) or LSI (large-scale integration) circuit.

The chip, when applied in a semiconductor device, is typically secured to a board and then sealed in a plastic

package or the like, so as to provide protection to the chip from its external environment and allow easy handling of the chip during use.

An example is taken here to describe an arrangement of a packaged semiconductor device having a chip with a transistor-integrated circuit (integrated circuit).

Figure 19 is an explanatory drawing showing a conventional arrangement of a packaged semiconductor device 101. The semiconductor device 101 is of a flipped-chip mounting type wherein the chip 102 is positioned so that its front faces the board 103. A package 108 made of epoxy resin is provided to cover the back of the chip 102, thereby sealing the chip 102.

The chip 102 is secured to the board 103 interposed by glue (anisotropic conducting glue) 105. The board 103 is made of glass epoxy prepared by immersing epoxy resin in glass fiber.

On the front of the chip 102 is there provided a pad section 107 as well as an integrated circuit (not shown). The pad section 107 has a bump 104 to establish contact to a wire section 106 made of copper film on the board 103.

Now, a typical method of manufacturing such a packaged semiconductor device will be described.

First, the wire section 106 with output wiring for

external connection is provided on the board 103 at a position that matches the position of the pad section 107 on the chip 102.

Then, a bump 104 is fabricated of gold on the pad section 107 of the chip 102, followed by application of glue 105 onto the board 103.

The board 103 and chip 102 are stacked so that the wire section 106 matches the bump 104 (pad section 107) in position, thereby mounting the chip 102 on the board 103.

Thereafter, the chip 102 and board 103 are compressed and secured to each other, while heating at about 200 °C. The glue 105 solidifies due to the heating, securing the chip 102 onto the board 103. The chip 102 is sealed by epoxy resin to form the package 108.

Generally, the chip 102 has a thickness of 200 μm or more. Besides, normally, the chip 102 is secured level (flat) onto the board 103 to retain its electrical properties.

Specific examples are disclosed about this kind of method of manufacturing a semiconductor device in Japanese Laid-Open Patent Application No. 11-238750/1999 (Tokukaihei 11-238750; published on August 31, 1999), Japanese Laid-Open Patent Application No. 64-15957/1989 (Tokukaisho 64-15957; published on January 19, 1989), and

other documents.

Tokukaihei No. 11-238750 discloses a method of manufacturing a highly reliable semiconductor device of a flipped-chip mounting type by removing residual scum from a vicinity of the pad section on the chip and improving the adherence between the pad section (metal) and the bump (metal).

Tokukaisho No. 64-15957 discloses a method of seal an NMOS type (N-type metal oxide semiconductor) element chip in a semiconductor package with a gas and liquid, whereby a mechanical pressure (stress) is applied to the chip using a gas and liquid so as to increase current flow for improved performance of the NMOS element.

Japanese Laid-Open Patent Application No. 5-93659/1993 (Tokukaihei 5-93659; published on April 16, 1993) discloses a distortion sensor which works by means of a stress being applied to various kinds of resistor elements, which is a technology not directly related to semiconductor elements, but rather to Tokukaisho No. 64-15957. The distortion sensor takes advantage of a glass layer which changes its electric resistance when distorted.

Incidentally, the semiconductor device 101 of a flipped-chip mounting type of Figure 19 has a structure that does not readily allow observation of the integrated

circuit provided on the front of the chip 102.

In other words, as mentioned above, the board 103 is secured on the front of the chip 102 interposed by the glue 105. Therefore, unsealing the epoxy resin package 108 covering the back of the chip 102 permits only a look at the back of the chip 102, allowing no observation or analysis of the structure of the integrated circuit.

However, the epoxy resin forming the board 103, the anisotropic conducting glue 105, etc. are removable using an etchant containing fuming nitric acid or sulfuric acid, for example. Therefore, the board 103 and glue 105 can be peeled off (removed) by the use of the etchant, separating the chip 102 from all the other parts. The chip 102, once separated, is prone to any kind of analysis; the integrated circuit on the front can be observable, and its electrical properties are measurable by directly contacting probes.

Further, the chip 102 secured level onto the board 103 in the package 108, i.e., packaged, has a thickness of 200 μm or more. Therefore, the chip 102 continues to be level even after it is separated from the all the other parts for analysis; the integrated circuit on the chip 102 operates normally exhibiting the same electrical properties as when it is packaged.

In short, the conventional semiconductor device 101,

when the epoxy resin is peeled to separate the chip 102 from all the other parts, is highly prone to analysis on its integrated circuit and other parts due to its arrangement and package method. This gives a rise to a problem that secrets cannot be well concealed.

Here, Tokukaihei 11-238750 and Tokukaisho 64-15957 mentioned above disclose technologies to improve the performance of the chip, but completely fails to pay attention to methods prohibiting the analysis of the chip (integrated circuit). These technologies still allow separation of the chip from all the other parts for analysis of the integrated circuit or other members.

Tokukaihei 5-93659 above, relating to a distortion sensor, belongs basically to a different field of technology from the present invention and neither discloses nor suggests the protection of the chip from analysis.

SUMMARY OF THE INVENTION

The present invention has an object to offer a semiconductor device which can completely prevent analysis of the integrated circuit of the semiconductor element secured to the board, as well as a method of manufacturing such a semiconductor device, i.e., to offer a semiconductor device which ensures protection of

secrets about the semiconductor element, as well as a method of manufacturing such a semiconductor device.

In order to achieve the object, a semiconductor device in accordance with the present invention includes a semiconductor element, with an integrated circuit, secured to a board, is such that the semiconductor element is secured level and specified to operate normally only when the semiconductor element is level.

According to the arrangement, the semiconductor element is specified to operate normally only when it is level. Therefore, if the semiconductor element is no longer capable of sustaining its level shape as a result of, for example, detachment of the semiconductor element from the board, the semiconductor element does not operate normally due to a resultant change and the like in its electrical properties. This ensures that any analysis is prohibited from being conducted on the integrated circuit on the semiconductor element. Thus, secrets can be concealed safely about the semiconductor element.

In order to achieve the object, a method of manufacturing a semiconductor device in accordance with the present invention includes, after securing a semiconductor element with an integrated circuit to a board so as to be level, the step of processing at least

a part of a back of the semiconductor element to develop such stress that when the semiconductor element is detached from the board, at least a part thereof deforms.

According to the arrangement, the semiconductor element is given such stress that when the semiconductor element is detached from the board, at least a part thereof deforms. Therefore, if the semiconductor element is detached from the board and can no longer sustain its level shape, the semiconductor element does not operate normally due to a resultant change and the like in its electrical properties. This ensures that any analysis is prohibited from being conducted on the integrated circuit on the semiconductor element. Thus, a semiconductor device can be manufactured in which secrets can be concealed safely about the semiconductor element.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1(a) is a cross-sectional view schematically showing an arrangement of a semiconductor device of a first embodiment in accordance with the present invention.

Figure 1(b) is a cross-sectional view showing the semiconductor device of Figure 1(a) which has deformed due to removal of a semiconductor element chip from it.

Figure 2 is a plan view schematically showing an arrangement of the semiconductor element chip of Figure 1(b).

Figure 3 is a circuit diagram showing, as an example, an arrangement of a distortion sensor provided in a sensor section, a transistor provided in a transistor section, and an LSI circuit provided in a LSI circuit section of a semiconductor element chip of Figure 1(b).

Figure 4, in reference to an example of a manufacturing process of the semiconductor device of Figure 1(a), is a cross-sectional view showing the semiconductor element chip being secured to a board.

Figure 5, in reference to an example of a manufacturing process of the semiconductor device of Figure 1(a), is a cross-sectional view showing the semiconductor element chip being processed on its back.

Figure 6, in reference to an example of a manufacturing process of the semiconductor device of Figure 1(a), is a cross-sectional view showing the semiconductor element chip having been processed on its back.

Figure 7, in reference to an example of a manufacturing process of the semiconductor device of Figure 1(a), is a cross-sectional view showing the semiconductor element chip having been packaged.

Figure 8(a) is a cross-sectional view schematically showing an arrangement of a semiconductor device of a second embodiment in accordance with the present invention.

Figure 8(b) is a cross-sectional view showing the semiconductor device of Figure 8(a) which has deformed due to removal of a semiconductor element chip from it.

Figure 9(a) is an explanatory drawing showing a pre-processing arrangement of the semiconductor element chip of Figure 8(b).

Figure 9(b) is a cross-sectional view showing the semiconductor element chip of Figure 8(b) which has distorted.

Figure 10(a) is an explanatory drawing schematically showing an arrangement of a semiconductor device of a third embodiment in accordance with the present invention.

Figure 10(b) is a cross-sectional view showing the semiconductor device of Figure 10(a) which has deformed due to removal of a semiconductor element chip from it.

Figure 11 is a plan view schematically showing an

arrangement of a lead frame in the semiconductor device of Figure 10(a).

Figure 12, in reference to an example of a manufacturing process of the semiconductor device of Figure 10(a), is a cross-sectional view showing the semiconductor element chip having been secured to a die pad.

Figure 13, in reference to an example of a manufacturing process of the semiconductor device of Figure 10(a), is a cross-sectional view showing the semiconductor element chip having been processed on its back.

Figure 14, in reference to an example of a manufacturing process of the semiconductor device of Figure 10(a), is a cross-sectional view showing the semiconductor element chip having been packaged.

Figure 15 is a cross-sectional view schematically showing an arrangement of a conventional semiconductor device of a wire bonding type.

Figure 16 is a plan view schematically showing an arrangement of a lead frame of the semiconductor device of Figure 15.

Figure 17 is a graph showing measurements of relationships between the thickness and warp (degrees of warp) of wafers (made of chip base material) which have

been thinned down from their original thickness of 725 μm by polishing.

Figure 18 is a graph showing measurements of relationships between amounts of etching and warp of wafers whose polished surfaces have been wet etched.

Figure 19 is a cross-sectional view schematically showing an arrangement of a conventional semiconductor device of a flipped-chip mounting type.

DESCRIPTION OF THE EMBODIMENTS

A semiconductor device in accordance with the present invention (hereinafter, "the present semiconductor device") has a semiconductor element with an integrated circuit.

The semiconductor element is secured level onto a board in, for example, a package.

The semiconductor element is specified to operate normally only when it is level. Conversely, the semiconductor element is specified to, when it becomes no longer capable of continuing to be level, cause a change in electrical or other properties of its transistor and integrated circuit and fail to operate normally.

Further, according to the specifications, the semiconductor element is receiving a stress (static stress) as a result of processing carried out on at least

a part of its back and, when detached from the board in the present semiconductor device, becomes no longer capable of continuing to be level and deforms (e.g., warps) at least partially due to the stress.

For these specifications, when the semiconductor element is separated from all the other parts and removed from the present semiconductor device, it deforms due to the stress and becomes no longer capable of continuing to be level, failing to operate normally.

Since the present semiconductor device is specified in this manner, when the semiconductor element is detached from the board, the semiconductor element deforms and changes its electrical and other properties, thereby being prevented from operating normally. The semiconductor element, when detached, can be thus protected from property and circuit analysis.

The present semiconductor device must be mounted to an external circuit when used. The present invention has an object to exploit, for various purposes, such a phenomenon that transistors, ICs (integrated circuits), and LSI (large-scale integration) circuits change their electrical properties when deformed; one of the purposes is to provide protection to the semiconductor element from analysis. The sensors and mounting methods which will be described in the following embodiments constitute

mere examples.

Note that in the present invention, "the semiconductor element being detached from the board" refers to the condition in which at least a part of the semiconductor element has peeled off the board.

[Embodiment 1]

A first embodiment in accordance with the present invention will be now described. Note that the scope of the present invention is by no means limited to this embodiment.

Referring to Figure 1(a), a semiconductor device 1 of the present embodiment is packaged, i.e., includes a semiconductor element chip (semiconductor element; hereinafter, "chip") 2 which is sealed in a package 8.

The semiconductor device 1 is of a flipped-chip mounting type whereby the chip 2 is positioned so that its front faces a board 3. The package 8 made of epoxy resin or other material is provided in a manner to cover the chip 2 on its back, thereby sealing the chip 2.

The board 3, formed from a glass epoxy board, has a wire section 6 made from copper foil on its side which contacts to the chip 2. The board 3 is fabricated by, for example, immersing epoxy resin in glass fiber.

The chip 2 is a silicon-made semiconductor element

chip and is secured onto the board 3 by a glue (anisotropic conducting glue) 5.

On the front of the chip 2 there are provided an electronic circuit section which will be described later and a pad section 7. The pad section 7 has a bump 4 to establish contact to a wire section 6 on the board 3.

The back 2a of the chip 2 is subjected to rough surface processing to apply a stress to the chip 2 to deform the chip 2. Due to the processing of the back 2a, the chip 2 warps due to stress when removed from the package 8 (when detached from the board 3) as shown in Figure 1(b).

A typical conventional semiconductor element has a thickness of 200 μm or more. By contrast, the chip 2 in the semiconductor device 1 has a thickness of 50 μm or less, preferably 30 μm to 50 μm, because of the rough surface processing. The chip 2 is therefore thinner entirely than conventional semiconductor elements and more prone to deformation caused by the stress applied to the processed back 2a when detached from the board 3.

An electronic circuit section provided on the front of the chip 2 will be now described.

Figure 2 is an explanatory drawing showing an arrangement of the electronic circuit section. As shown in Figure 2, the electronic circuit section includes a

transistor section 21, a sensor section 22 and an LSI circuit section 23.

The transistor section 21 is a part where transistors (of an NMOS type (N-type metal oxide semiconductor)) are provided at high density. The sensor section 22 is a part where a detector section (detector means; will be detailed later) is provided to detect electrical properties of the transistors. The LSI circuit section 23 is a part where circuitry including an IC (integrated circuit) or LSI (large-scale integration) circuit is provided.

The transistor in the transistor section 21 is specified to exhibit electrical properties according to the shape of the transistor section 21. In other words, the transistor possesses different electrical properties when the transistor section 21 is level (normal period) and when the transistor section 21 is deformed (deformed period).

When the chip 2 is detached from the board 3 and has warped convexly due to stress, the transistor section 21 provided on the front of the chip 2 warps accordingly. The semiconductor device 1 is therefore specified so that when the chip 2 is detached from the board 3, the transistor in the transistor section 21 changes its electrical property.

Now, changes in electrical properties of an NMOS transistor will be described which occur when the transistor section 21 deforms.

A stress (external force) was applied to the transistor section 21, for example, so that it warped convexly in a direction perpendicular to current flow through the transistor and normal to the front of the chip 2, and as a result, the front of the transistor section 21 actually warped due to the stress, forming a warped surface having a radius (r) of 10 mm. In these circumstances, the transistor, when activated, showed a 10 % increase in its channel current.

In this manner, the transistor is specified to change its electrical properties according to the shape of the transistor section 21.

The detector section in the sensor section 22 is for detecting an electrical properties of the transistor in the transistor section 21 and controlling the LSI circuit provided in the LSI circuit section 23 according to results of the detection.

In other words, the detector section is specified to activate the LSI circuit if it detects an electrical property exhibited by the transistor at normal period (exhibited by the transistor provided in a level part of the transistor section 21) and to deactivates the LSI

circuit if it detects an electrical property exhibited by the transistor at deformed period.

In this manner, the semiconductor device 1 is specified so that the detector section detects a change in electrical properties (current, voltage, etc.) of the transistor caused by the warp of the chip 2 (transistor section 21) to utilize the results in the control of the operation of the LSI circuit.

As the detector section may OP-amplifier or another analog circuit be used for example. The OP-amplifier is for detecting a change in electrical properties of the transistor which occurs when the level transistor section 21 deforms.

Now, referring to Figure 3, a concrete arrangement example will be now described of the electronic circuit section, especially the distortion sensor, in the chip 2. As shown in Figure 3, the electronic circuit section includes a transistor 24, a distortion sensor 25, and an LSI circuit 26.

The distortion sensor 25 is an OP-amplifier with a resistor R and a comparator Cp, acting as the aforementioned detector section. As shown in Figure 3, in the distortion sensor 25, the resistor R is connected at one of its ends to the transistor 24 in the transistor section 21 (see Figure 2) and grounded at the other end.

The comparator Cp has two input terminals and an output terminal. One of the input terminals is connected to a wire connecting the resistor R to the transistor 24. A predetermined voltage V_2 is applied in advance to the other input terminal. The output terminal is connected to the LSI circuit 26 in the LSI circuit section 23 (see Figure 2).

In these circumstances, the predetermined voltage V_2 is equal to or exceeds the characteristic voltage V_1 of the transistor 24 at normal period and is specified lower than the characteristic voltage V_1 of the transistor 24 at deformed period.

The characteristic voltage V_1 refers to a voltage the transistor 24 generates when it receives a drive voltage. As the transistor 24 receives a drive voltage, it outputs a characteristic current I_d which changes in value according to the shape of the transistor section 21. The value of the characteristic voltage V_1 is determined by the characteristic current I_d and the resistor R connected to the transistor 24.

As describe earlier, the characteristic current I_d of the transistor 24 increases in value as the transistor section 21 warps, which means that the characteristic voltage V_1 increases as the transistor section 21 warps.

The comparator Cp compares the characteristic

voltage V_1 with the predetermined voltage V_2 to determine which voltage is higher. According to its specifications, the comparator Cp outputs low signal (operation signal) from its output terminal to the LSI circuit 26 if the characteristic voltage V_1 is either lower than or equal to the predetermined voltage V_2, and conversely, outputs high signal to the LSI circuit 26 if the characteristic voltage V_1 is higher than the predetermined voltage V_2.

The LSI circuit 26 has an operation prohibition circuit 27 for controlling the operation of the LSI circuit 26 itself according to an output signal of the distortion sensor 25 (comparator Cp).

The operation prohibition circuit 27 allows the LSI circuit 26 to operate when it receives low signal from the distortion sensor 25. Meanwhile, the operation prohibition circuit 27 is specified to prohibit the operation of the LSI circuit 26 when it receives high signal or no signal at all from the distortion sensor 25. To put it differently, according to specifications, the LSI circuit 26 is allowed to operate only when it receives low signal from the distortion sensor 25.

Next, the operation of the electronic circuit section in accordance with conditions of the chip 2 (transistor section 21) will be described.

At normal period, i.e., when the chip 2 is secured

to the board 3 and packaged so that the transistor section 21 is level (normal conditions), the transistor 24 exhibits normal electrical properties. Therefore, the predetermined voltage V_2 is equal to or exceeds the characteristic voltage V_1 ($V_1 \leq V_2$), causing the comparator Cp in the distortion sensor 25 to output low signal to the LSI circuit 26. The LSI circuit 26 hence operates normally.

By contrast, when the package 8 of the semiconductor device 1 is opened and the chip 2 is detached from the board 3, as shown in Figure 1(b), the chip 2 (and the transistor section 21) warps convexly due to stress.

The electrical properties of the transistor 24 thereby change, and the transistor 24 outputs a characteristic current I_d at an increased value. Consequently, the characteristic voltage V_1 becomes greater than the predetermined voltage V_2 ($V_1 > V_2$), and the comparator Cp in the distortion sensor 25 outputs high signal to the LSI circuit 26. Receiving the high signal, the operation prohibition circuit 27 causes the LSI circuit 26 to stop operating.

As described above, in the semiconductor device 1, the chip 2 is secured level onto the board 3 (with the chip being flipped). Further, the chip 2 is specified to, when detached from the board 3, deform due to the stress

which develops as a result of the rough surface processing carried out on the back 2a.

The chip 2 specified to operate normally when it is level and to fail to operate normally when it has deformed. In other words, in the chip 2, as the distortion sensor 25 detects changes in electrical properties of the transistor 24 caused by deformation, the operation prohibition circuit 27 stops the LSI circuit 26 from operating.

This ensures that in the semiconductor device 1, any analysis is prohibited from being conducted on the LSI circuit 26 of the chip 2 when the chip 2 is detached from the board 3. Thus, secrets can be concealed safely about the chip 2.

As mentioned earlier, the LSI circuit 26 is specified to be prohibited by the operation prohibition circuit 27 from operating when it receives no signal. Therefore, the LSI circuit 26 is not operable alone (when detached from the LSI circuit section 23); in these conditions, no analysis of the circuit is ever possible by means of probing.

Now, a method of manufacturing the semiconductor device 1 will be described.

First, a chip 2 having a thickness of 200 μm or more is prepared, including a pad section 7. A wire section 6

with output wiring for external connection is then provided on the board 3 at a position that matches the position of the pad section 7 of the chip 2. This is followed by fabrication of a bump 4 of gold on the pad section 7 of the chip 2.

As shown in Figure 4, glue (anisotropic conducting glue) 5 is applied on the board 3. Thereafter, the board 3 and chip 2 are stacked so that the wire section 6 matches the bump 4 (pad section 7) in position, thereby mounting the chip 2 on the board 3.

Next, the chip 2 and board 3 are compressed and secured to each other, while heating at about 200 °C. The glue 5 solidifies due to the heating, securing the chip 2 onto the board 3. By these steps, the chip 2 is mounted in a flipped posture to be level on the board 3.

The board 3 on which the chip 2 is secured is loaded at a predetermined position in a dicing machine. The back 2a of the chip 2 is scraped (subjected to rough surface processing) entirely using a dicing blade 9 provided in the dicing machine as shown in Figure 5 and Figure 6.

The scraping is carried out to reduce the thickness of the chip 2 to 50 μm or less, preferably to a range of 30 μm to 50 μm.

In addition, the scraping of the back 2a by means of the dicing blade 9 is preferably carried out in a

specified direction (for example, in a direction normal to the paper showing Figure 5). Thus, the back 2a of the chip 2 is shaped by the scraping so that the chip 2 readily deforms due to stress.

The scrape processing carried out on the entirety of the back 2a renders the chip 2 entirely thinner, enabling predetermined stress to be applied to the chip 2 entirely.

Next, as shown in Figure 7, the chip 2 is sealed by epoxy resin using a predetermined mold to form a package 8. The manufacture of the semiconductor device 1 is hence completed.

In this manner, the chip 2 has its back 2a subjected to rough surface processing and therefore, has such a structure that once it is detached from the board 3 and deforms due to stress, it does not easily return to the level shape.

The structure thereby never allows the chip 2 to completely return to the level shape even by, for example, vacuum adsorption on a level base. To put it differently, the chip 2, once deformed, by no means completely returns to the level shape. Nor can any analysis be conducted on the LSI 26 and other circuits, once the chip 2 is deformed, as described earlier.

Note that the chip 2 is scraped after being mounted

in a flipped posture. Therefore, the chip 2 can retain its level shape inside the semiconductor device 1 even when it is thinned down and receives stress.

The scrape processing by means of the dicing blade 9 produces no adverse effects on devices, such as the transistor 24 and LSI circuit 26 in the chip 2, which we confirmed through experiments and other methods.

The scraping by means of the dicing blade 9 is preferably carried out so as to render the steps formed by the dicing (groove pitches formed by the scraping) as short as possible. Short steps would enable a stress to be applied to the chip 2 easily.

Further, prior to the scraping by means of the dicing blade 9, the chip 2 may be thinned down entirely to some extent (for example, about 50 μm) by a typical scrape or other method, as required.

In the present embodiment, it is specified that the scraping of the back 2a of the chip 2 using the dicing blade 9 is carried out in a specified direction (for example, in a direction normal to the paper showing Figure 5); however, the scraping may be carried out in whichever direction that results in easy deformation of the chip 2 due to stress or may be carried out in two or more different directions.

In the present embodiment, it is specified that the

steps formed by the scraping are rendered as short as possible; however, the scraping requires no particular limitations.

In the present embodiment, it is specified that the dicing blade 9 is used in the rough surface processing of the entire back 2a of the chip 2; however, there are no particular limitations as to which part(s) of the chip 2 is(are) to be thinned down. Only the transistor section 21 may be thinned down, for example.

However, the chip 2 is specified to detect electrical properties of the transistor 24 using the distortion sensor 25, as described earlier. Therefore, the chip 2 is preferably thinned down in such a manner that at least the transistor section 21 deforms due to stress.

The present embodiment only refers to a case where the back 2a of the chip 2 is entirely scraped by dicing; however, the back 2a of the chip 2 may be scraped by a method other than dicing. Examples include physical scraping by means of sand blast or sandpaper and treatment by means of laser beam projection.

Scraping methods other than dicing will be now described.

If the back 2a of the chip 2 is to be treated by means of a laser as an example, prior to the treatment,

the chip 2 is thinned down to some extent (for example, about 50 μm) by a typical scrape or other method.

The board 3 on which the chip 2 is secured is loaded in a predetermined place in a laser marker device (laser beam projection device). The laser beam is preferably a converging laser beam which is a focused energy beam. Specifically, such a converging laser beam can be generated by means of, for example, a laser light source using YAG (yttrium aluminum garnet) as a solid laser medium.

The back 2a of the chip 2 is treated by projection of a laser beam with, for example, the second harmonic wavelength of 532 nm. As a result of the treatment, numerous minute dents or irregularities are formed on the back 2a, enabling a predetermined stress to be applied to the chip 2.

There are no particular limitations on the wavelength of the laser beam or requirements in the projection. However, the laser beam with the above specified wavelength produces no adverse effects to devices, such as the transistor 24 and LSI circuit 26 of the chip 2, which we confirmed through experiments and other methods.

If the back 2a of the chip 2 is to be scraped by means of sand blast as another example, prior to the

scraping, the chip 2 is thinned down to some extent similarly to the foregoing case.

The board 3 on which the chip 2 is secured is loaded in a predetermined place in a sand blast processing device, and the back 2a of the chip 2 is scraped so that the chip 2 has a thickness of, for example, 50 μm or less, preferably in a range of 30 μm to 50 μm. For the scraping, calcium carbonate particles of, for example, #1000 (about 15 μm) are preferably used as sand blast particles (grind particles).

As a result of the scrape processing, numerous minute dents or irregularities are formed on the back 2a, enabling a predetermined stress to be applied to the chip 2.

There are no particular limitations on the kind of the sand blast particles or requirements in the scraping. However, the calcium carbonate particles produce no adverse effects to devices, such as the transistor 24 and LSI circuit 26 of the chip 2, which we confirmed through experiments and other methods.

Alternatively, if the back 2a of the chip 2 is to be manually scraped by means of sandpaper as another example, prior to the scraping, the chip 2 is thinned down to some extent similarly to the foregoing cases.

The back 2a of the chip 2 is scraped using sandpaper

so that the chip 2 has a thickness of, for example, 50 μm or less, preferably in a range of 30 μm to 50 μm. As a result of the scrape processing, numerous minute dents or irregularities are formed on the back 2a, enabling a predetermined stress to be applied to the chip 2.

There are no particular requirements in the scraping using sandpaper. However, the use of sandpaper of a relatively large particle size is preferable, since it would enable easy application of stress to the chip 2. The use of sandpaper produces no adverse effects to devices, such as the transistor 24 and LSI circuit 26 of the chip 2, which we confirmed through experiments and other methods.

The scraping by means of sandpaper is carried out manually and requires good attention. However, it is the easiest processing method.

[Embodiment 2]

A second embodiment in accordance with the present invention will be now described. Here, for convenience, members of the present embodiment that have the same function as members of the first embodiment, and that are mentioned in that embodiment are indicated by the same reference numerals and description thereof is omitted.

Figure 8(a) is an explanatory drawing showing an

arrangement of a semiconductor device 11 of the present embodiment. As shown in this Figure, the semiconductor device 11 is different from the semiconductor device 1 in that the chip 2 is replaced with a chip 12.

As shown in Figures 1(a) and 1(b), the chip 2 in the semiconductor device 1 has its back 2a subjected to rough surface processing. By contrast, as shown in Figures 8(a) and 8(b), the chip 12 in the semiconductor device 30 is has a part of its back 12a subjected to the rough surface processing.

Specifically, as shown in Figures 9(a) and 9(b), only a part of the back 12a of the chip 12, that is, the back side of the transistor section 21 (the part of the back 12a opposite to the transistor section 21) is subjected to rough surface processing. Only this part is thinned down, with the others remaining the same.

Therefore, the chip 12 is thinned down in the transistor section 21 (for example, to 50 μm or less) and remains at the same thickness in the sensor section 22 and LSI circuit section 23 (for example, 200 μm or more).

Therefore, the chip 12 receives stress only in the transistor section 21 and deforms only in the transistor section 21 due to stress when detached from the board 3.

As described here, as to the chip 12, only a part of the back 12a (transistor section 21) is subjected to